12-Bit, 105MSPS Analog-To-Digital Converter

FEATURES

- 12-Bit Resolution
- 105MSPS Sample Rate
- High SNR: 70dBFS at 100MHz f_{IN}
- High SFDR: 86dBc at 100MHz f_{IN}
- 2.3V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3V Single-Supply Voltage
- Analog Power Dissipation: 571mW
  - Output Buffer Power: 165mW
- Pin-Compatible with:
  ADS5500 (14-Bit, 125MSPS)
  ADS5541 (14-Bit, 105MSPS)
  ADS5542 (14-Bit, 80MSPS)
  ADS5520 (12-Bit, 125MSPS)
  ADS5522 (12-Bit, 80MSPS)
- TQFP-64 PowerPAD™ Package
- Recommended Op Amps:
  THS3201, THS3202, THS4503, THS4509,
  THS9001, OPA695, OPA847

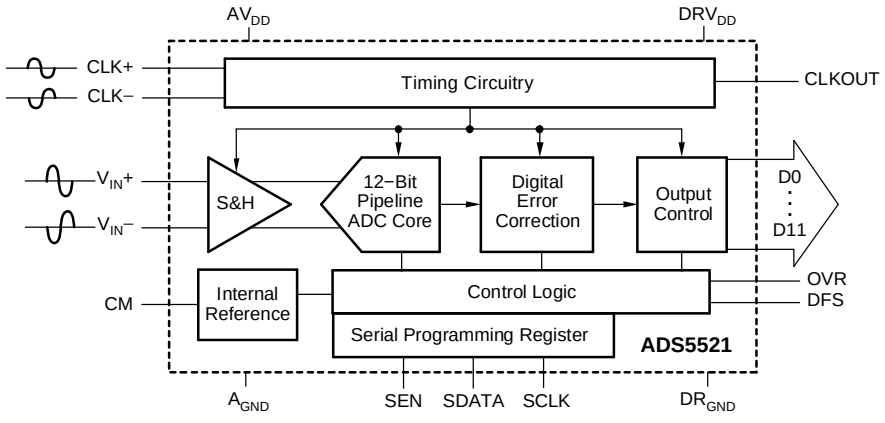
APPLICATIONS

- Wireless Communication
  - Communication Receivers
  - Base Station Infrastructure
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
  - Radar
  - Infrared
- Video and Imaging
- Medical Equipment
- Military Equipment

DESCRIPTION

The ADS5521 is a high-performance, 12-bit, 105MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in very little space, the ADS5521 has excellent analog power dissipation of 571mW and output buffer power dissipation of 165mW from a 3.3V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. Parallel CMOS-compatible output ensures seamless interfacing with common logic.

The ADS5521 is available in a 64-pin TQFP PowerPAD package and is pin-compatible with the ADS5500, ADS5541, ADS5542, ADS5520, and ADS5522. This device is specified over the full temperature range of –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5521	HTQFP-64(2) PowerPAD	PAP	–40C to +85C	ADS5521I	ADS5521IPAP	Tray, 160
					ADS5521IPAPR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum, or see the TI web site at www.ti.com.
(2) Thermal pad size: 3.5mm x 3.5mm (min), 4mm x 4mm (max). θ_{JA} = 21.47°C/W and θ_{JC} = 2.99°C/W, when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard, four-layer, 3 in x 3 in PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		ADS5521	UNIT
Supply Voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}	–0.3 to +3.7	V
	A_{GND} to DR_{GND}	±0.1	V
Analog input to A_{GND}		–0.3 to minimum (AVDD + 0.3, 3.6)	V
Logic input to DR_{GND}		–0.3 to DRV_{DD}	V
Digital data output to DR_{GND}		–0.3 to DRV_{DD}	V
Operating temperature range		–40 to +85	°C
Junction temperature		+105	°C
Storage temperature range		–65 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
Supplies					
Analog supply voltage, AV_{DD}		3.0	3.3	3.6	V
Output driver supply voltage, DRV_{DD}		3.0	3.3	3.6	V
Analog input					
Differential input range			2.3		V_{PP}
Input common-mode voltage, V_{CM}(1)		1.45	1.55	1.65	V
Digital Output					
Maximum output load			10		pF
Clock Input					
ADCLK input sample rate (sine wave) $1/t_C$	DLL ON	60		105	MSPS
	DLL OFF	2		80	MSPS
Clock amplitude, sine wave, differential(2)		1	3		V_{PP}
Clock duty cycle(3)			50		%
Open free-air temperature range		–40		+85	°C

(1) Input common-mode should be connected to CM.
(2) See Figure 48 for more information.
(3) See Figure 47 for more information.

ELECTRICAL CHARACTERISTICS

Typical values given at T_A = +25°C, min and max specified over the full temperature range of –40°C to +85°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				12		Bits
Analog Inputs						
Differential input range				2.3		V_{PP}
Differential input capacitance	See Figure 39			4		pF
Analog input common-mode current (per input)				250		µA
Analog input bandwidth	Source impedance = 50Ω			750		MHz
Voltage overload recovery time				4		Clock cycles
Internal Reference Voltages						
Reference bottom voltage, V_{REFM}				1.0		V
Reference top voltage, V_{REFP}				2.15		V
Reference error			–4	±0.9	+4	%
Common-mode voltage output, V_{CM}			1.50	1.55	1.60	V
Dynamic DC Characteristics and Accuracy						
No missing codes				Tested		
Differential nonlinearity error, DNL	f_{IN} = 55MHz		–0.5	±0.25	+0.5	LSB
Integral nonlinearity error, INL	f_{IN} = 55MHz		–1.5	±0.55	+1.5	LSB
Offset error				±1.5		mV
Offset temperature coefficient				0.02		%/°C
DC power-supply rejection ratio, DC PSRR	Δoffset error/ΔAV_{DD} from AV_{DD} = 3.0V to AV_{DD} = 3.6V			0.25		mV/V
Gain error				±0.3		%FS
Gain temperature coefficient				–0.02		Δ%/°C
Dynamic AC Characteristics						
Signal-to-noise ratio. SNR	f_{IN} = 10MHz			71		dBFS
	f_{IN} = 55MHz	+25°C to +85°C	68.0	70.5		dBFS
		Full temp range	66.8	69.0		dBFS
	f_{IN} = 70MHz			70.3		dBFS
	f_{IN} = 100MHz			70.0		dBFS
	f_{IN} = 150MHz			69.3		dBFS
	f_{IN} = 220MHz			67.8		dBFS
RMS idle channel noise	Input tied to common-mode			0.32		LSB
Spurious-free dynamic range, SFDR	f_{IN} = 10MHz			83.0		dBc
	f_{IN} = 55MHz	Room temp	78.0	86.0		dBc
		Full temp range	76.0	85.0		dBc
	f_{IN} = 70MHz			81.0		dBc
	f_{IN} = 100MHz			86.0		dBc
	f_{IN} = 150MHz			75.0		dBc
	f_{IN} = 220MHz			72.0		dBc

ELECTRICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, min and max specified over the full temperature range of –40°C to +85°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Second-harmonic, HD2	f_{IN} = 10MHz			90.0		dBc
	f_{IN} = 55MHz	Room temp	78.0	86.0		dBc
		Full temp range	76.0	85.0		dBc
	f_{IN} = 70MHz			81.0		dBc
	f_{IN} = 100MHz			88.0		dBc
	f_{IN} = 150MHz			75.0		dBc
	f_{IN} = 220MHz			72.0		dBc
Third-harmonic, HD3	f_{IN} = 10MHz			83.0		dBc
	f_{IN} = 55MHz	Room temp	78.0	88.0		dBc
		Full temp range	76.0	87.0		dBc
	f_{IN} = 70MHz			87.0		dBc
	f_{IN} = 100MHz			86.0		dBc
	f_{IN} = 150MHz			80.0		dBc
	f_{IN} = 220MHz			78.0		dBc
Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 55MHz			87.0		dBc
Signal-to-noise + distortion, SINAD	f_{IN} = 10MHz			70.7		dBFS
	f_{IN} = 55MHz	Room temp	67.0	70.0		dBFS
		Full temp range	65.8	68.5		dBFS
	f_{IN} = 70MHz			69.6		dBFS
	f_{IN} = 100MHz			69.3		dBFS
	f_{IN} = 150MHz			68.2		dBFS
	f_{IN} = 220MHz			65.8		dBFS
Total harmonic distortion, THD	f_{IN} = 10MHz			79.0		dBc
	f_{IN} = 55MHz	Room temp	76.0	83.0		dBc
		Full temp range	74.0	82.0		dBc
	f_{IN} = 70MHz			78.0		dBc
	f_{IN} = 100MHz			84.0		dBc
	f_{IN} = 150MHz			74.0		dBc
	f_{IN} = 220MHz			70.3		dBc
Effective number of bits, ENOB	f_{IN} = 55MHz			11.3		Bits
Two-tone intermodulation distortion, IMD	f = 10.1MHz, 15.1MHz (-7dBFS each tone)			94.6		dBFS
	f = 50.1MHz, 55.1MHz (-7dBFS each tone)			96.6		dBFS
	f = 150.1MHz, 155.1MHz (-7dBFS each tone)			84.7		dBFS

ELECTRICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, min and max specified over the full temperature range of –40°C to +85°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply					
Total supply current, ICC	f_{IN} = 55MHz		223	250	mA
Analog supply current, IAVDD	f_{IN} = 55MHz		173	185	mA
Output buffer supply current, IDRVDD	f_{IN} = 55MHz		50	65	mA
Power dissipation	Analog only		571	611	mW
	Output buffer power with 10pF load on digital output to ground		165	215	mW
Standby power	With Clocks running		180	250	mW

DIGITAL CHARACTERISTICS

Valid over full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3V, and $3V_{PP}$ differential clock, unless otherwise noted.

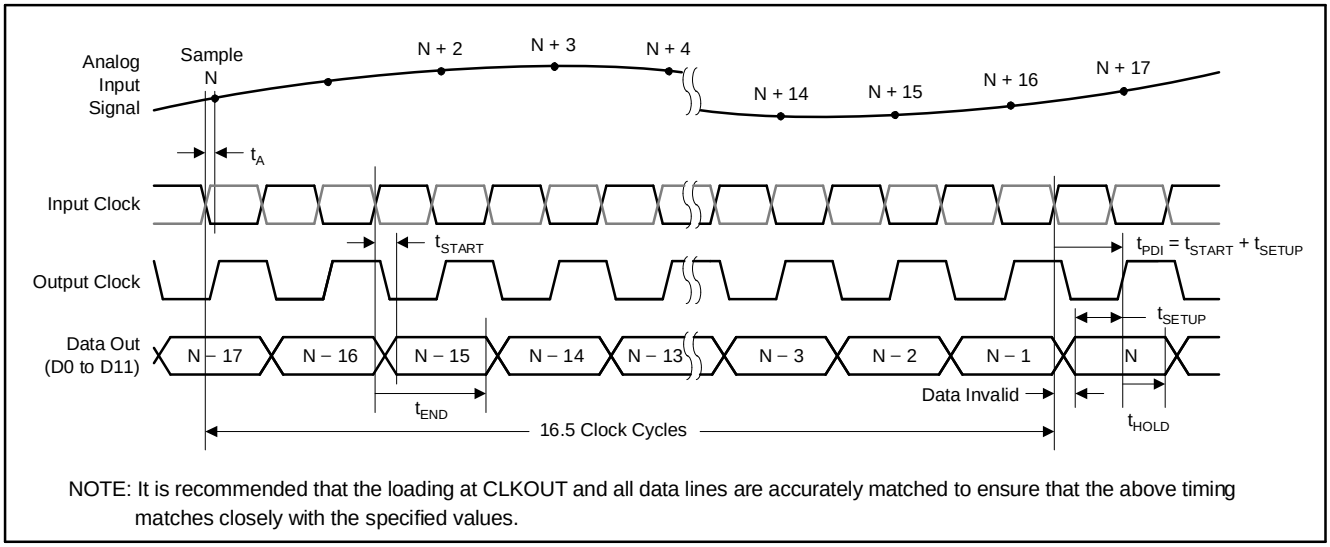
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs					
High-level input voltage, V_{IH}		2.4			V
Low-level input voltage, V_{IL}				0.8	V
High-level input current, I_{IH}				10	µA
Low-level input current, I_{IL}				10	µA
Input current for RESET			–20		µA
Input capacitance			4		pF
Digital Outputs					
Low-level output voltage, V_{OL}	C_{LOAD} = 10pF		0.3	0.4	V
High-level output voltage, V_{OH}	C_{LOAD} = 10pF	2.4	3.0		V
Output capacitance			3		pF

TIMING CHARACTERISTICS(1)(2)

Typical values given at T_A = +25°C, min and max specified over the full temperature range of –40°C to +85°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Aperture delay, t_A	Input CLK falling edge to data sampling point		1		ns
Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
Data setup time, t_{SETUP}	Data valid(3) to 50% of CLKOUT rising edge	2.2	2.8		ns
Data hold time, t_{HOLD}	50% of CLKOUT rising edge to data becoming invalid(3)	2.2	2.5		ns
Input clock to output data valid start, t_{START}(4)	Input clock rising edge to data valid start delay		1.9	2.8	ns
Input clock to output data valid end, t_{END}(4)	Input clock rising edge to data valid end delay	5.8	7.3		ns
Output clock jitter, t_{JIT}	Uncertainty in CLKOUT rising edge, peak-to-peak		175	250	ps_{PP}
Output clock rise time, t_{RISE}	Rise time of CLKOUT from 20% to 80% of DRV_{DD}		2.0	2.2	ns
Output clock fall time, t_{FALL}	Fall time of CLKOUT from 80% to 20% of DRV_{DD}		1.7	1.8	ns
Data rise time, t_r	Data rise time measured from 20% to 80% of DRV_{DD}		4.4	5.1	ns
Data fall time, t_f	Data fall time measured from 80% to 20% of DRV_{DD}		3.3	3.8	ns
Output enable(OE) to data output delay	Time required for outputs to have stable timings with regard to input clock(5) after OE is activated			1000	Clock cycles
Wakeup time	Time to valid data after coming out of software power down, after stopping and restarting the input clock			1000	Clock cycles

(1) Timing parameters are ensured by design and characterization, and not tested in production.
(2) See Table 5 through Table 8 in the *Application Information* section for timing information at additional sampling frequencies.
(3) Data valid refers to 2.0V for LOGIC HIGH and 0.8V for LOGIC LOW.
(4) Refer to the *Output Information* section for details on using the input clock for data capture.
(5) Data outputs are available within a clock from assertion of OE; however, it takes 1000 clock cycles to ensure stable timing with respect to input clock.



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 1. Timing Diagram

RESET TIMING CHARACTERISTICS

Typical values given at T_A = +25°C, min and max specified over the full temperature range of –40°C to +85°C, AV_{DD} = DRV_{DD} = 3.3V, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Power-on delay, t_1	Delay from power-on of AVDD and DRVDD to RESET pulse active	10			ms
Reset pulse width, t_2	Pulse width of active RESET signal	2			µs
Register write delay, t_3	Delay from RESET disable to SEN active	2			µs
Power-up time	Delay from power-up of AV_{DD} and DRV_{DD} to output stable		40		ms

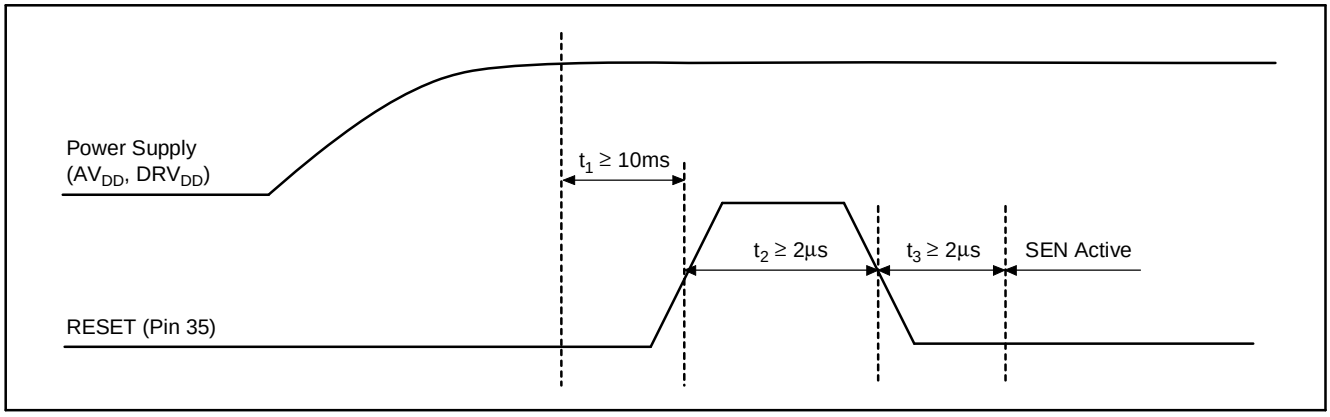


Figure 2. Reset Timing Diagram

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The ADS5521 has a three-wire serial interface. The ADS5521 latches serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at the falling edge.
- Minimum width of data stream for a valid loading is 16 clocks
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiples of 16-bit words within a single active SEN pulse.

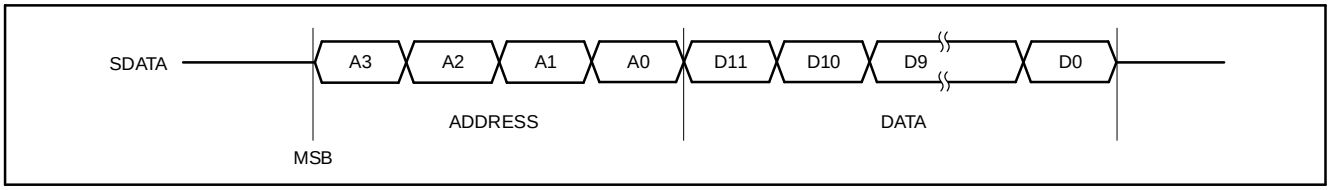


Figure 3. DATA Communication is 2-Byte, MSB First

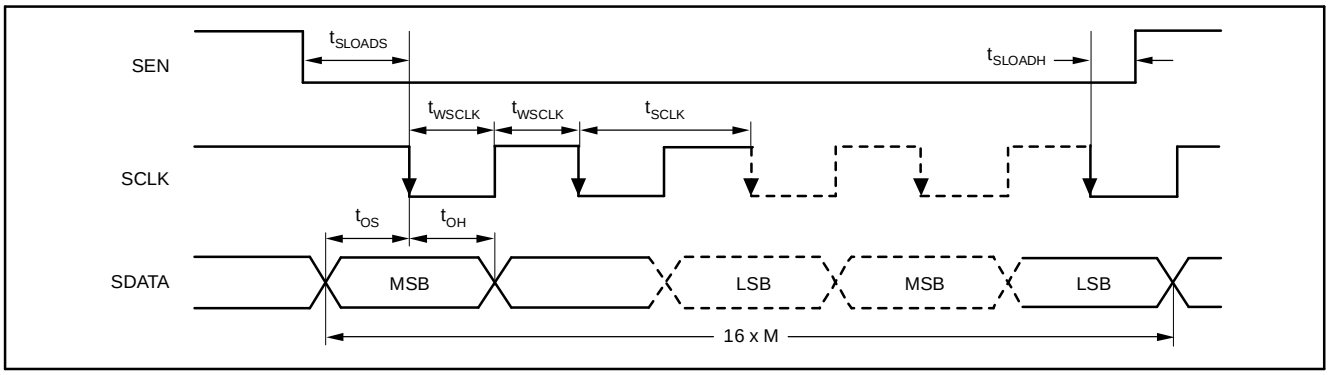


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface TIming Characteristics

SYMBOL	PARAMETER	MIN(1)	TYP(1)	MAX(1)	UNIT
t_{SCLK}	SCLK period	50			ns
t_{WSCLK}	SCLK duty cycle	25	50	75	%
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
t_{DS}	Data setup time	8			ns
t_{DH}	Data hold time	6			ns

(1) Typ, min, and max values are characterized, but not production tested.

Table 2. Serial Register Table(1)

A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	1	0	0	0	0	0	0	0	0	0	0	DLL OFF	0	DLL OFF = 0: Internal DLL is on; recommended for 60MSPS to 105MSPS clock speeds. DLL OFF = 1: Internal DLL is off; recommended for 2MSPS to 80MSPS clock speeds.
1	1	1	0	0	TP<1>	TP<0>	0	0	0	0	0	0	0	0	0	TP<1:0> - Test modes for output data capture TP<1:0> = 00: Normal mode of operation TP<1:0> = 01: All outputs forced to 0 TP<1:0> = 10: All outputs forced to 1 TP<1:0> = 11: Each output bit toggles between 0 and 1. There is no ensured relationship between the bits.(2)
1	1	1	1	PDN	0	0	0	0	0	0	0	0	0	0	0	PDN = 0: Normal mode of operation PDN = 1: Device is put in power-down (low-current) mode.

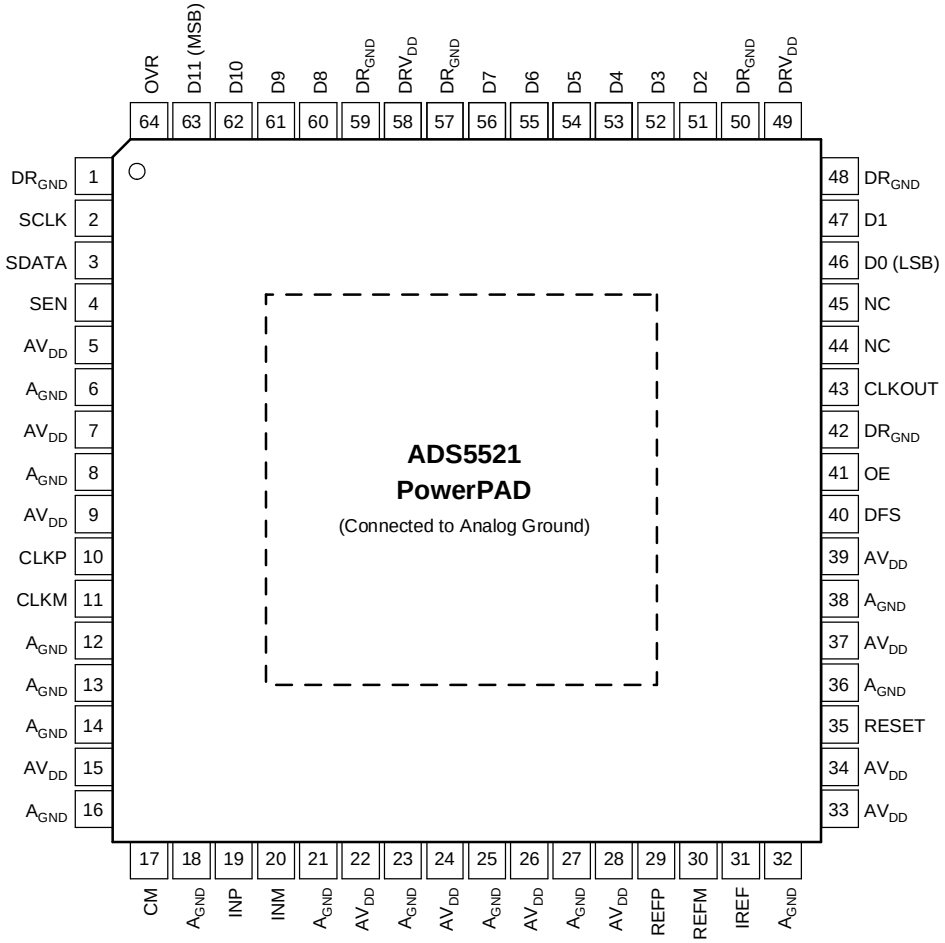
(1) All register contents default to zero on reset.
(2) The patterns given are applicable to the straight offset binary output format. If two's complement output format is selected, the test mode outputs will be the binary two's complement equivalent of these patterns.

Table 3. Data Format Select (DFS) Table

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{2}{12} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{4}{12} \times AV_{DD} < V_{DFS} < \frac{5}{12} \times AV_{DD}$	Two's Complement	Data valid on rising edge
$\frac{7}{12} \times AV_{DD} < V_{DFS} < \frac{8}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{10}{12} \times AV_{DD}$	Two's Complement	Data valid on falling edge

PIN CONFIGURATION

PAP PACKAGE
HTQFP-64
(TOP VIEW)



PIN CONFIGURATION (continued)

PIN ASSIGNMENTS(1)

TERMINAL		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AV_{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A_{GND}	6, 8, 12, 13, 14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV_{DD}	49, 58	2	I	Output driver power supply
DR_{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
NC	44, 45	2	—	Not connected
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 0.1µF capacitor in series with a 1Ω resistor to GND
REFM	30	1	O	Reference voltage (negative); 0.1µF capacitor in series with a 1Ω resistor to GND
IREF	31	1	I	Current set; 56kΩ resistor to GND; do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high), 200kΩ resistor to AV_{DD}
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select(2)
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select
SDATA	3	1	I	Serial interface data
SCLK	2	1	I	Serial interface clock
D0 (LSB) to D11 (MSB)	46, 47, 51-56, 60-63	14	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

(1) PowerPAD is connected to analog ground.
(2) Table 3 defines the voltage levels for each mode selectable via the DFS pin.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low frequency value.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the *Electrical Specifications* section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference ($T_{MAX} - T_{MIN}$).

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

TYPICAL CHARACTERISTICS

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

SPECTRAL PERFORMANCE (FFT for 4MHz Input Signal)

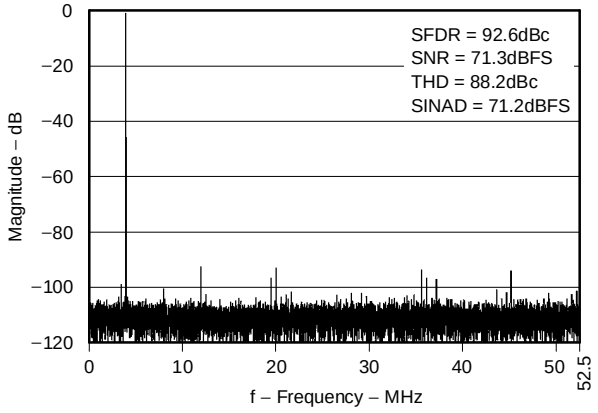


Figure 5.

SPECTRAL PERFORMANCE (FFT for 16MHz Input Signal)

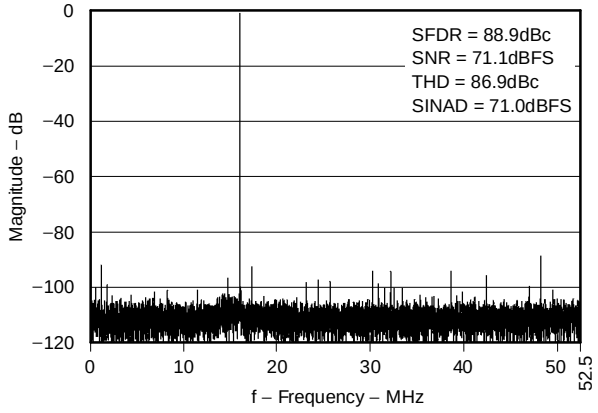


Figure 6.

SPECTRAL PERFORMANCE (FFT for 55MHz Input Signal)

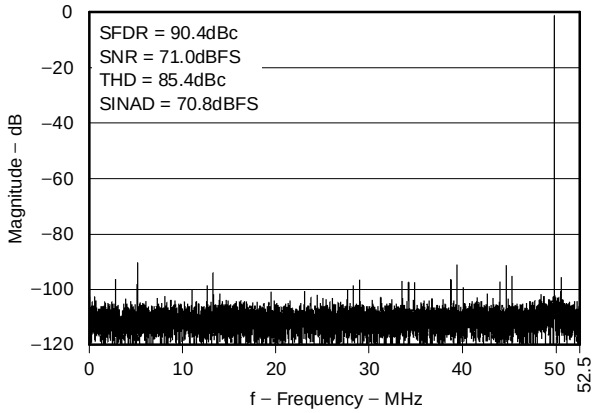


Figure 7.

SPECTRAL PERFORMANCE (FFT for 70MHz Input Signal)

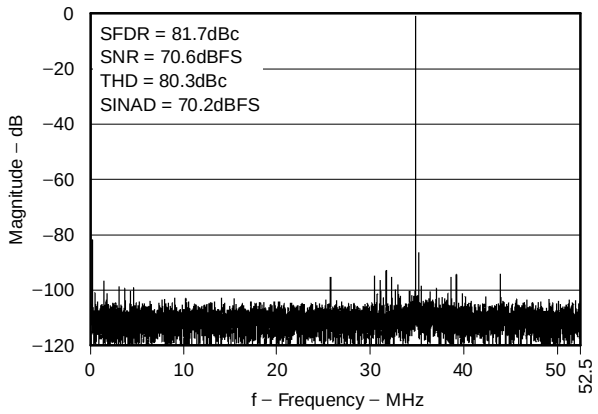


Figure 8.

SPECTRAL PERFORMANCE (FFT for 80MHz Input Signal)

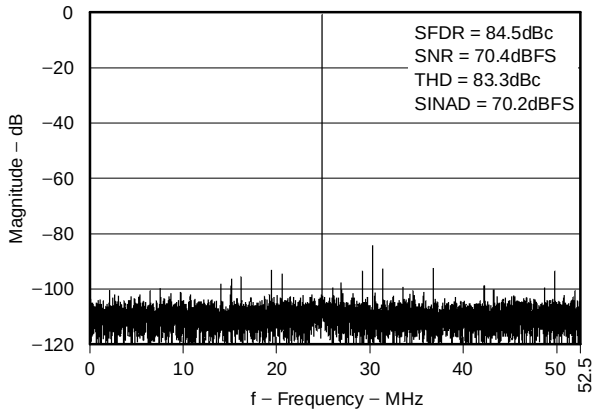


Figure 9.

SPECTRAL PERFORMANCE (FFT for 100MHz Input Signal)

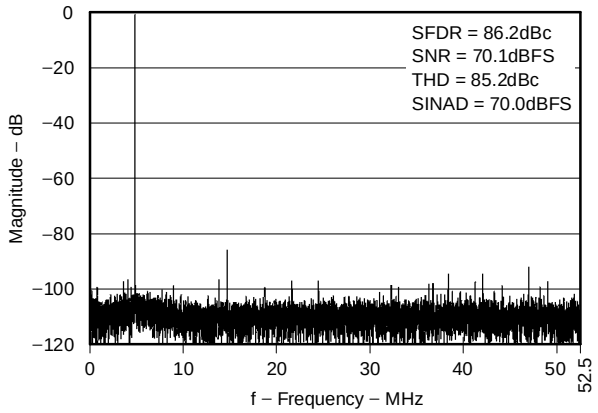


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

SPECTRAL PERFORMANCE (FFT for 150MHz Input Signal)

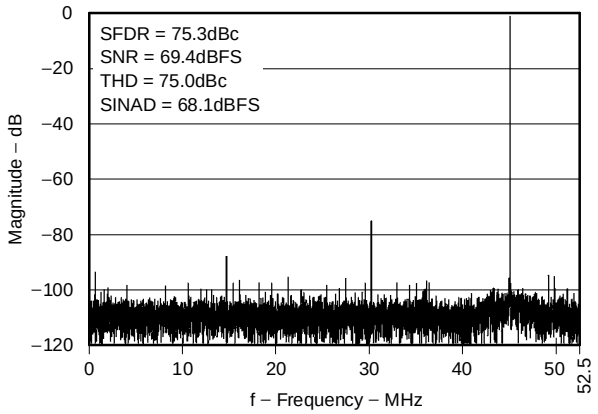


Figure 11.

SPECTRAL PERFORMANCE (FFT for 220MHz Input Signal)

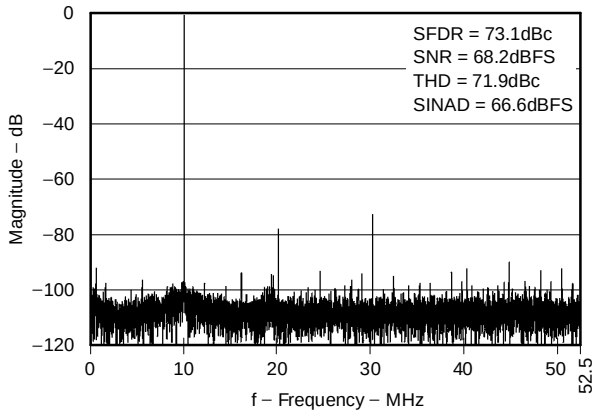


Figure 12.

SPECTRAL PERFORMANCE (FFT for 300MHz Input Signal)

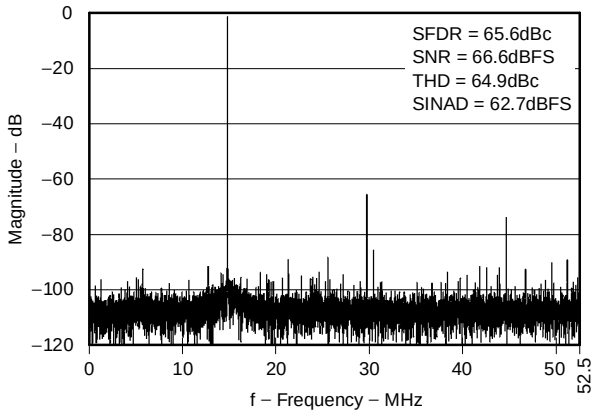


Figure 13.

TWO-TONE INTERMODULATION

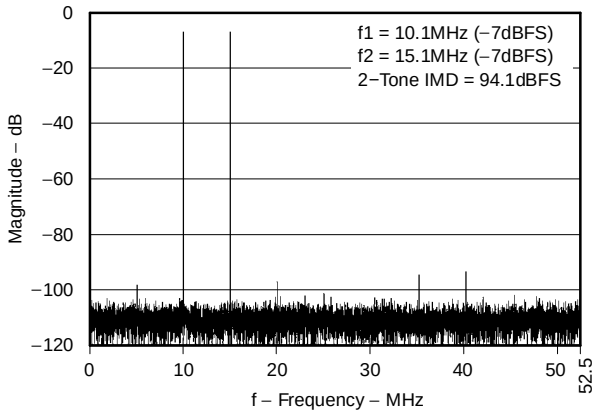


Figure 14.

TWO-TONE INTERMODULATION

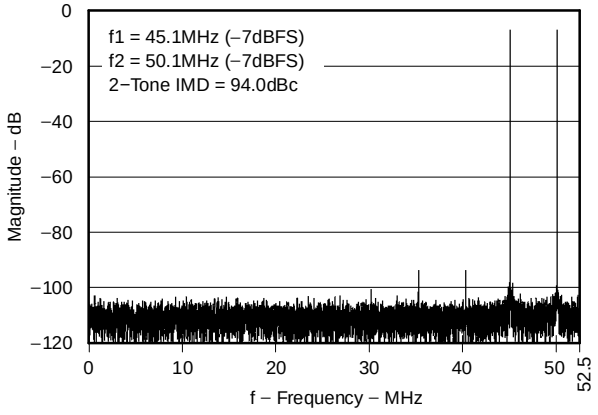


Figure 15.

TWO-TONE INTERMODULATION

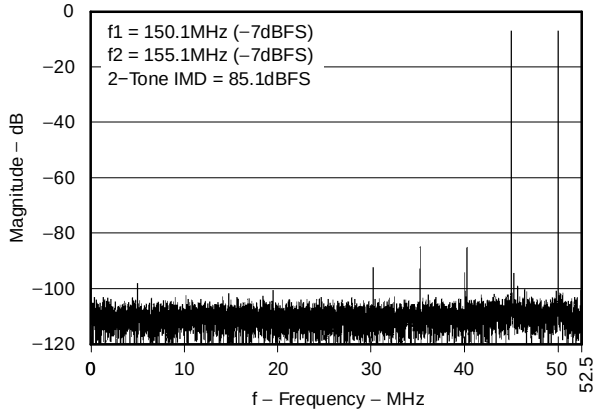


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

DIFFERENTIAL NONLINEARITY

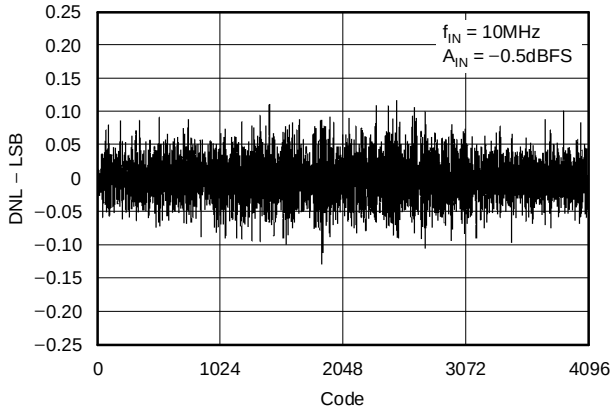


Figure 17.

INTEGRAL NONLINEARITY

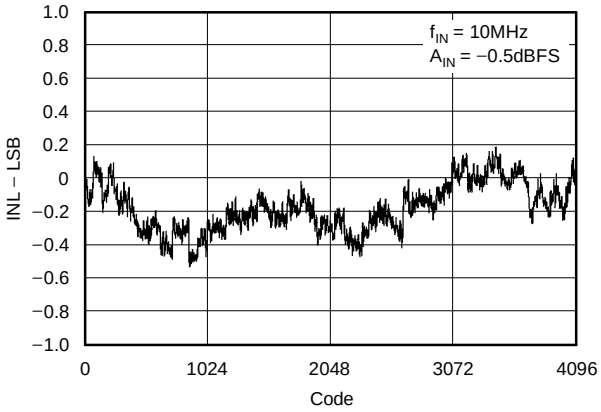


Figure 18.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

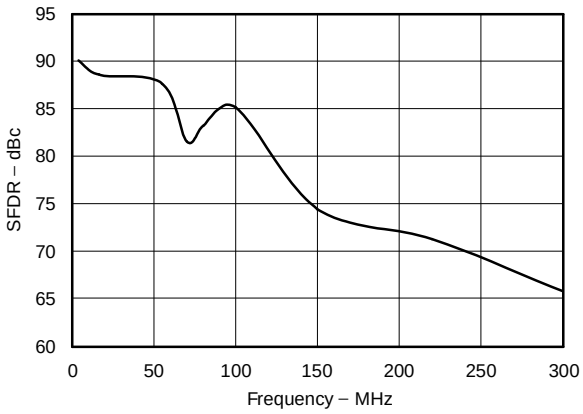


Figure 19.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

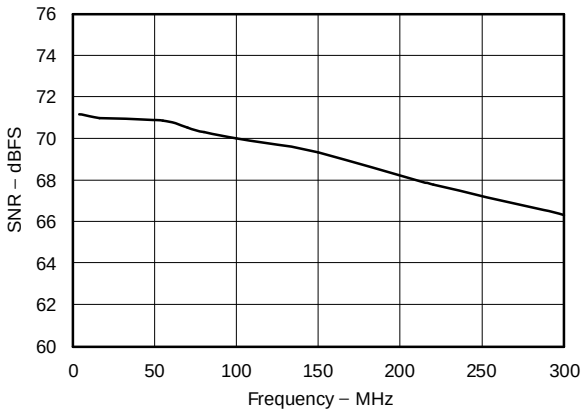


Figure 20.

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

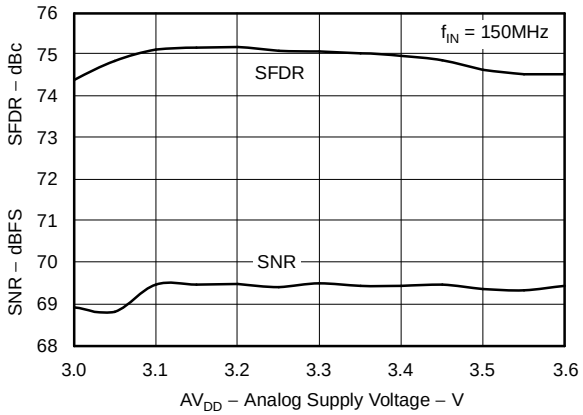


Figure 21.

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

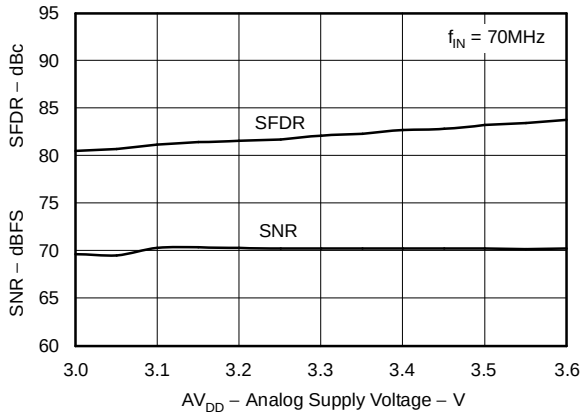


Figure 22.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

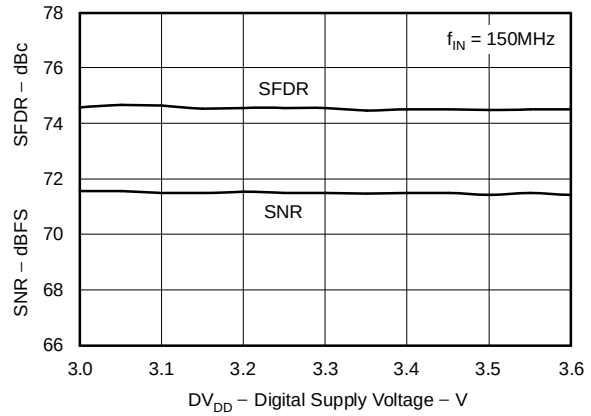


Figure 23.

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

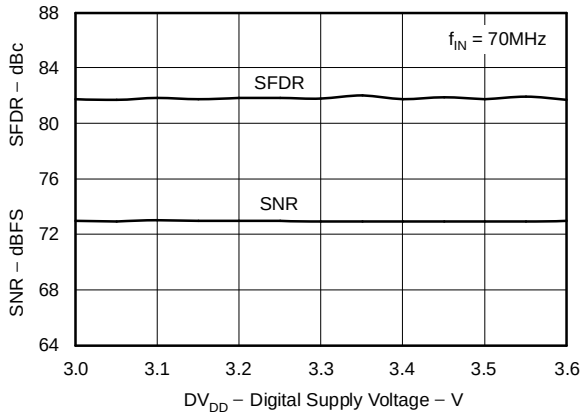


Figure 24.

POWER DISSIPATION vs SAMPLE RATE

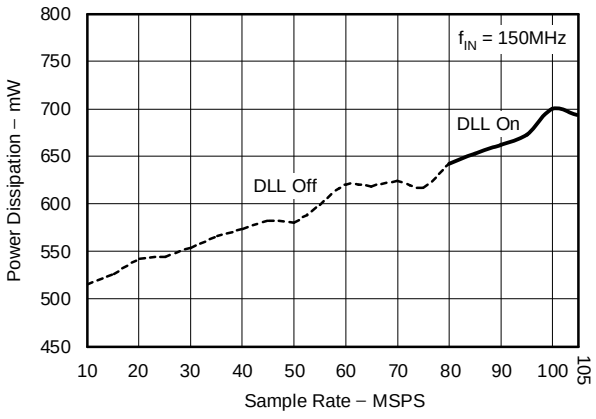


Figure 25.

POWER DISSIPATION vs SAMPLE RATE

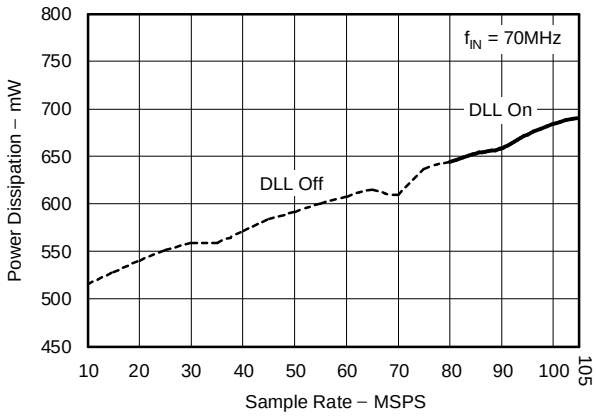


Figure 26.

AC PERFORMANCE vs TEMPERATURE

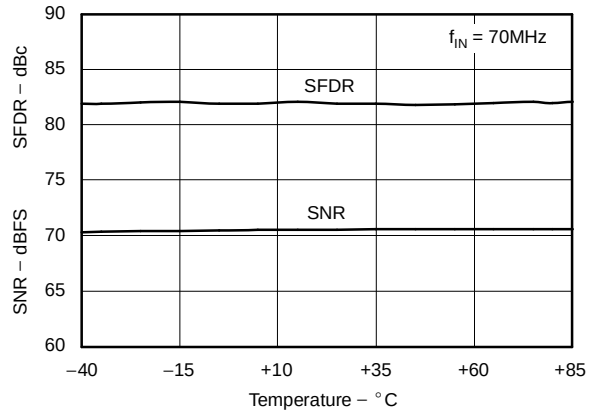


Figure 27.

AC PERFORMANCE vs INPUT AMPLITUDE

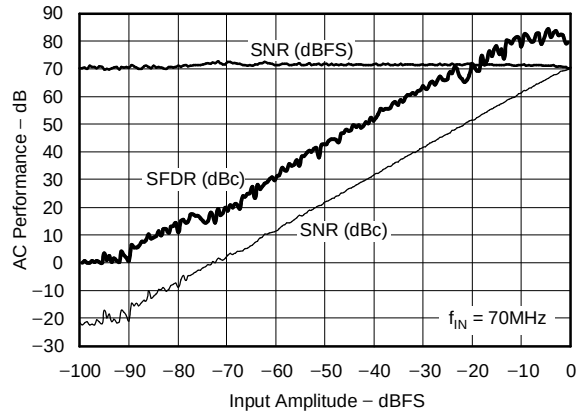


Figure 28.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, DLL On, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

AC PERFORMANCE vs INPUT AMPLITUDE

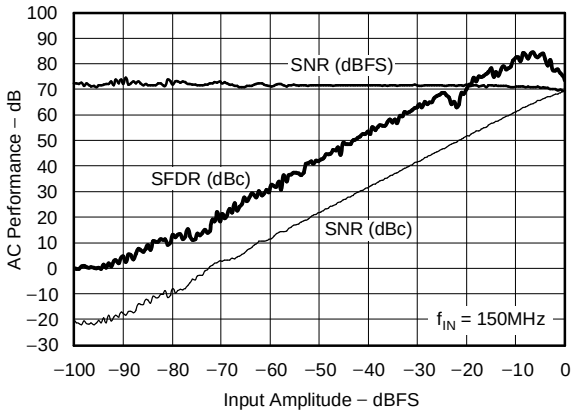


Figure 29.

AC PERFORMANCE vs INPUT AMPLITUDE

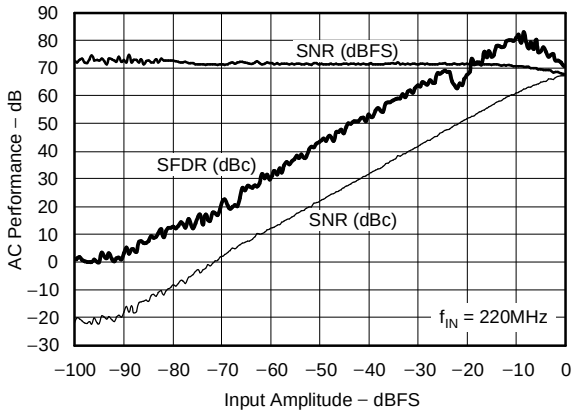


Figure 30.

OUTPUT NOISE HISTOGRAM

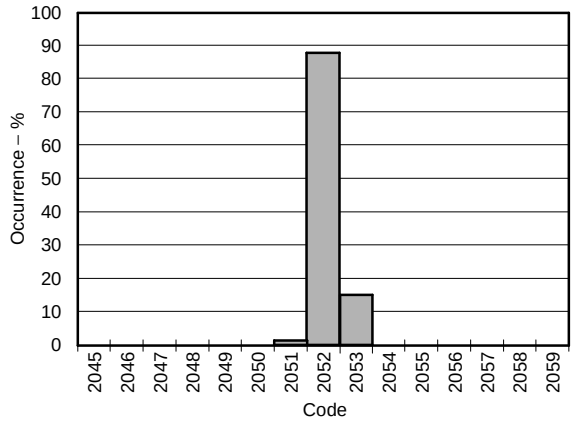


Figure 31.

AC PERFORMANCE vs CLOCK AMPLITUDE

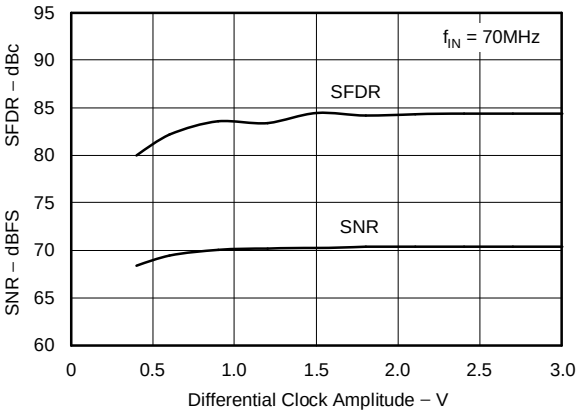


Figure 32.

WCDMA CARRIER

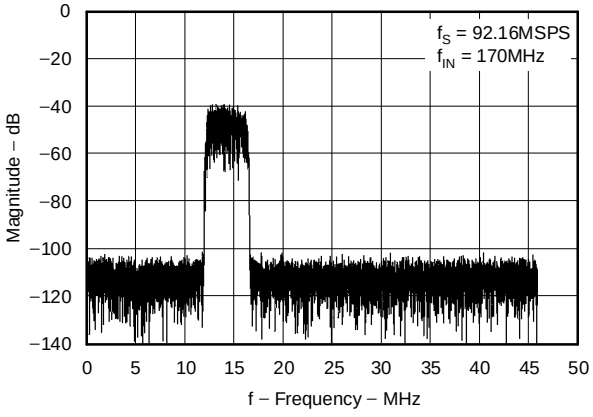


Figure 33.

AC PERFORMANCE vs CLOCK DUTY CYCLE

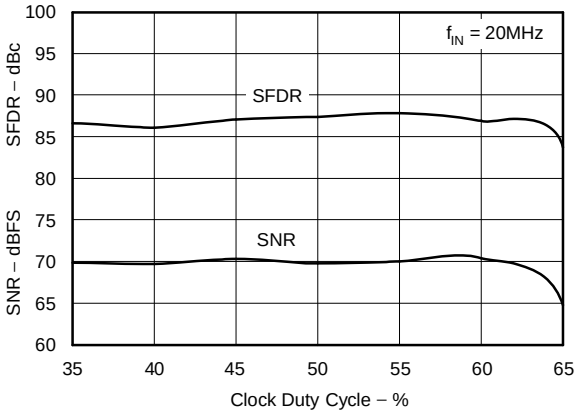


Figure 34.

TYPICAL CHARACTERISTICS

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

SIGNAL-TO-NOISE RATIO (SNR)
(DLL On)

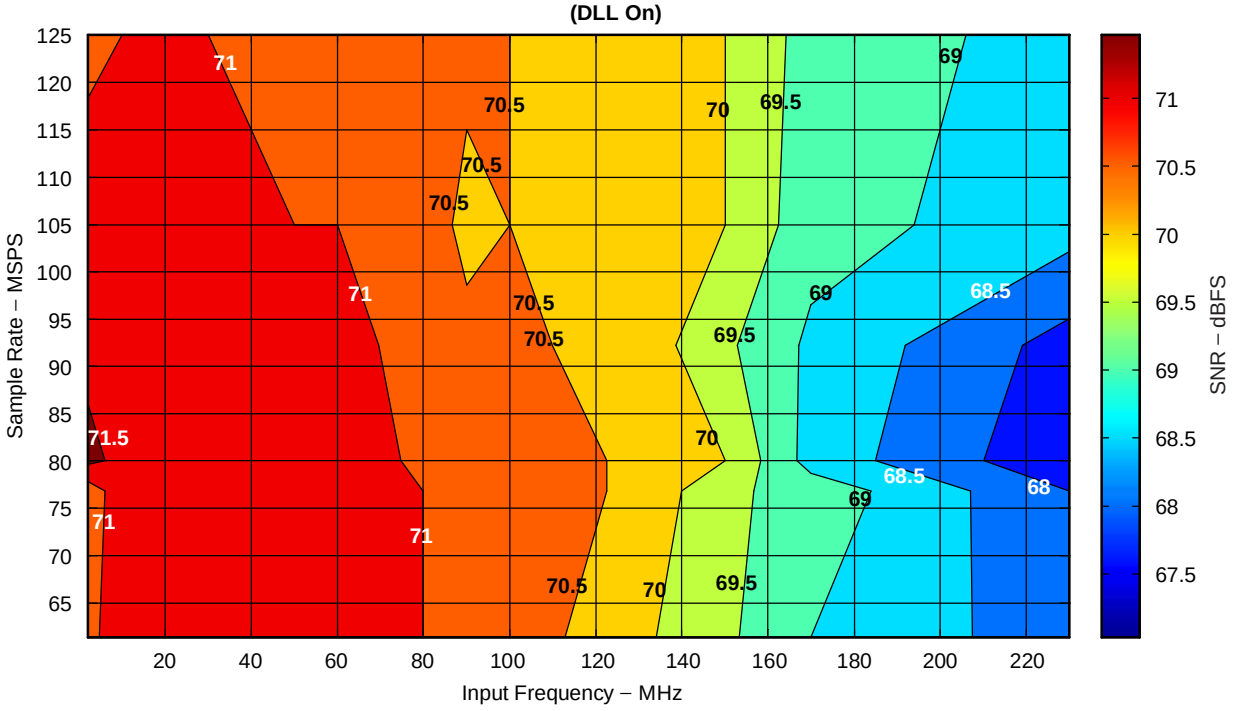


Figure 35.

SIGNAL-TO-NOISE RATIO (SNR)
(DLL Off)

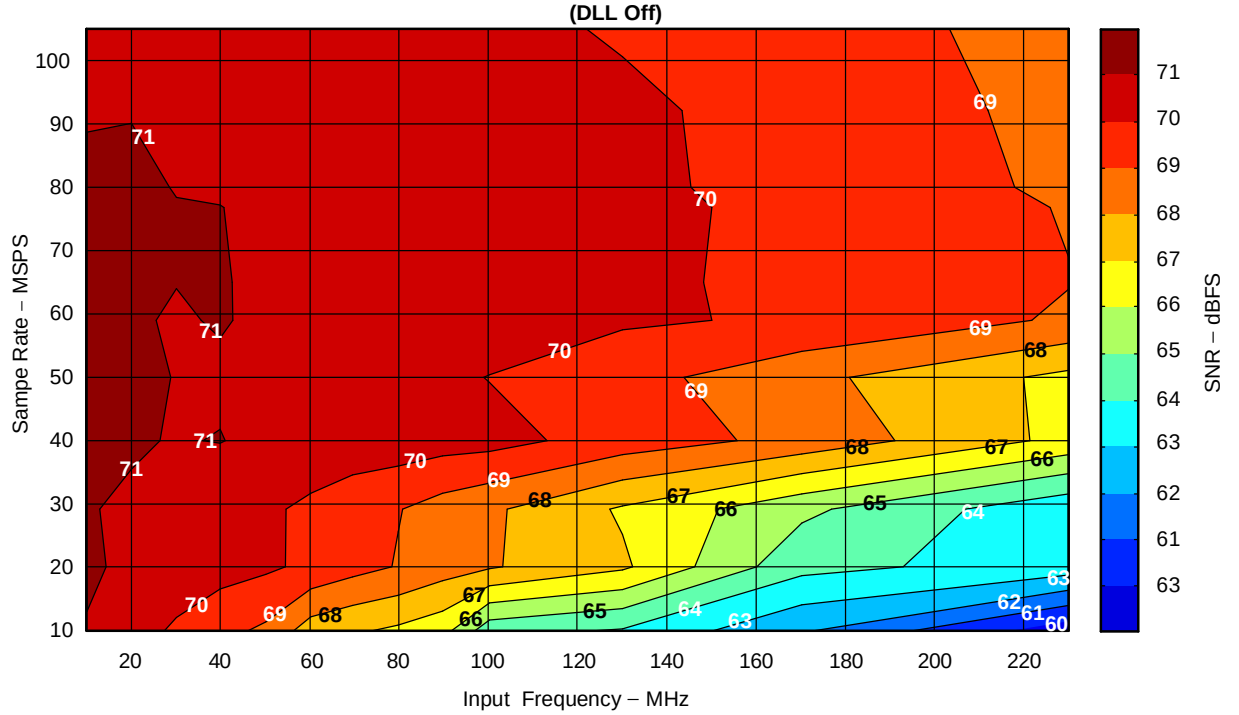


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = +25°C, AV_{DD} = DRV_{DD} = 3.3V, sampling rate = 105MSPS, 50% clock duty cycle, $3V_{PP}$ differential clock, and –1dBFS differential input, unless otherwise noted.

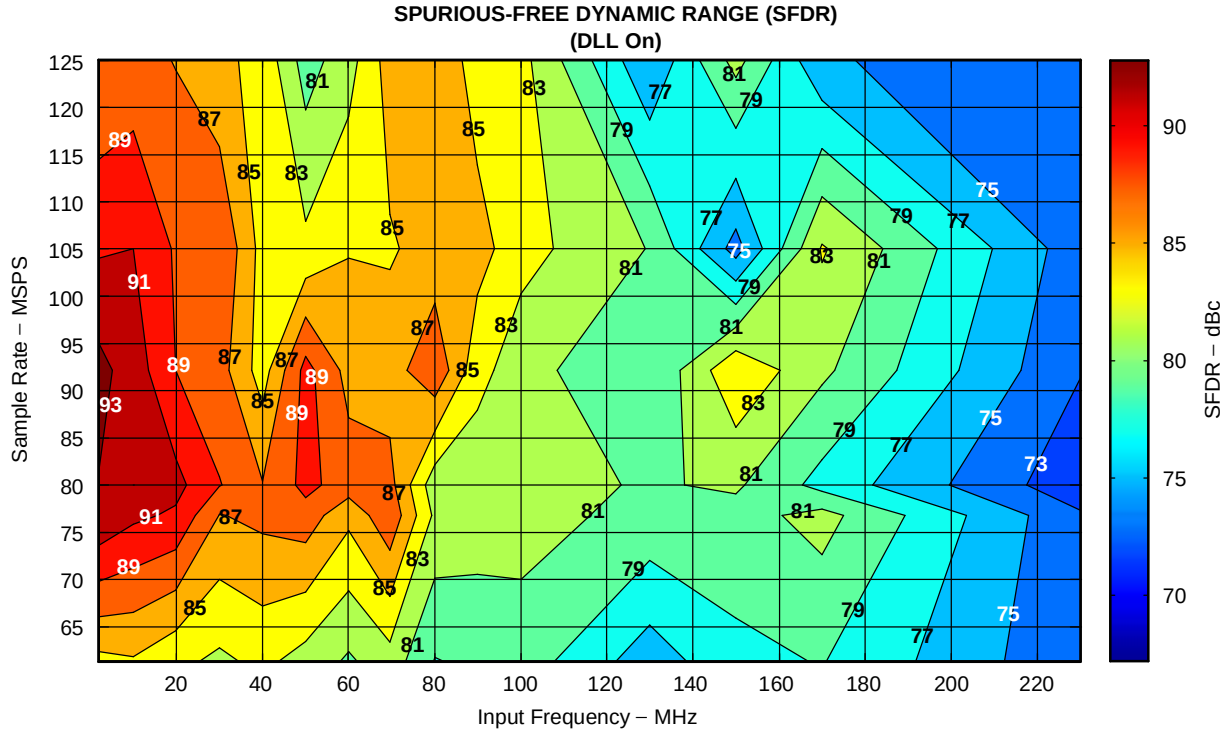


Figure 37.

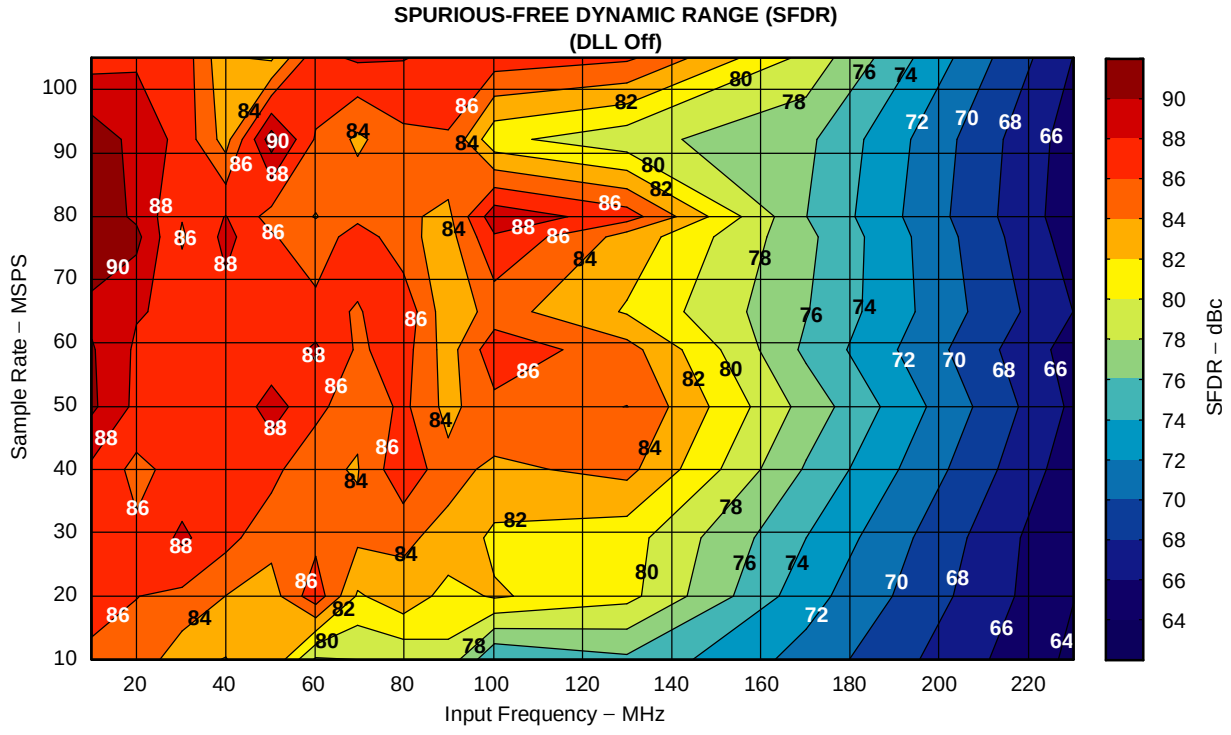


Figure 38.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5521 is a low-power, 12-bit, 105MSPS, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 16.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in either straight offset binary or binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5521 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique, shown in Figure 39.

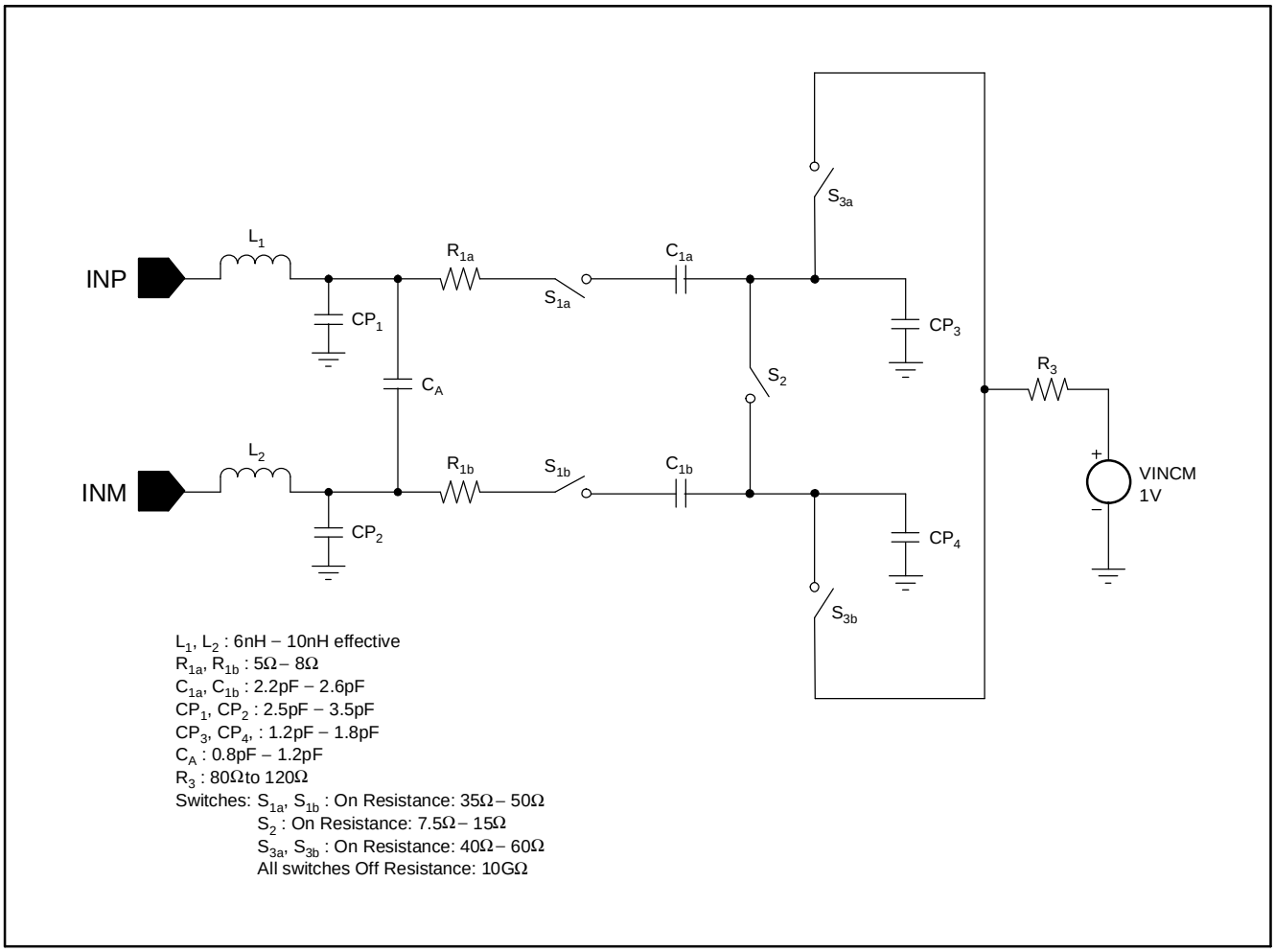


Figure 39. Analog Input Stage

This differential input topology produces a high level of AC performance for high sampling rates. It also results in a very high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5521 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between CM + 0.575V and CM – 0.575V. This means that each input is driven with a signal of up to CM ± 0.575V, so that each input has a maximum differential signal of $1.15V_{PP}$ for a total differential input signal swing of $2.3V_{PP}$. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5521 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 40 illustrates one possible configuration using an RF transformer.

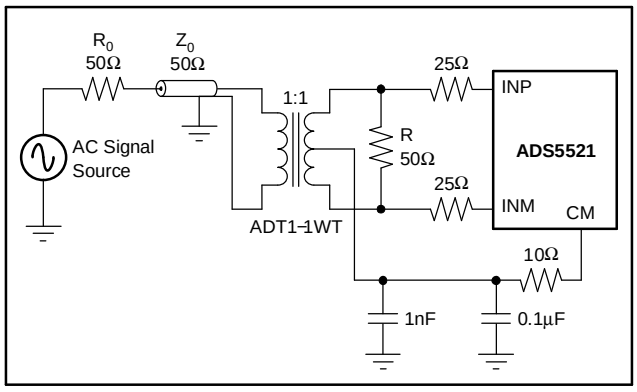


Figure 40. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Placing a 25Ω resistor in series with INP and INM is recommended to dampen ringing due to ADC kickback.

Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5521 is connected to the center-tap of the secondary winding.

To ensure a steady low-noise V_{CM} reference, best performance is attained when the CM output (pin 17) is filtered to ground with a 10Ω series resistor and parallel 0.1µF and 0.001µF low-inductance capacitors, as illustrated in Figure 39.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 500µA (250µA per input). Equation 1 describes the dependency of the common-mode current and the sampling frequency:

$$\frac{500\mu A \times f_S \text{ (in MSPS)}}{105 \text{ MSPS}} \quad (1)$$

Where:

f_S > 2MSPS.

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5521. TI offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA695, and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as TI's THS9001, can also be used with an RF transformer for very high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5521

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20MHz	THS4503	Differential In/Out Amp	No
DC to 50MHz	OPA847	Operational Amp	Yes
10MHz to 120MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100MHz	THS9001	RF Gain Block	Yes

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA695, or OPA847) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5521. These three amplifier circuits minimize even-order harmonics. For very high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5521 directly, as shown in Figure 40, or with the addition of the filter circuit shown in Figure 41.

Figure 41 illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5521 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5521 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring DC coupling of the input. Flexible in their configurations (see Figure 42), such amplifiers can be used for single-ended-to-differential conversion signal amplification.

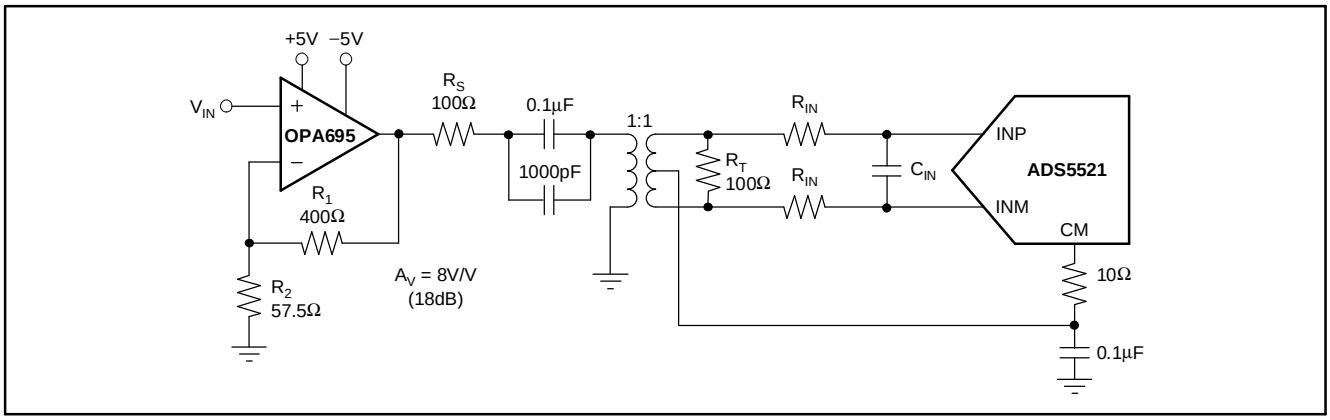


Figure 41. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

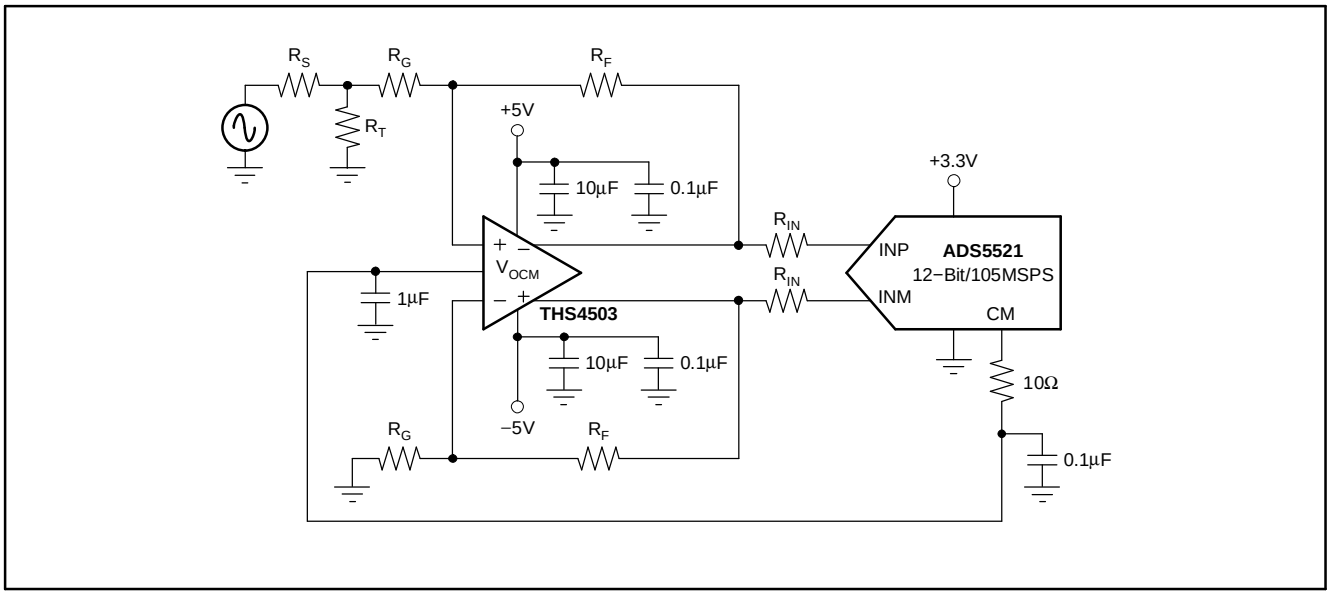


Figure 42. Using the THS4503 with the ADS5521

INPUT VOLTAGE OVER-STRESS

The ADS5521 can handle absolute maximum voltages of 3.6V DC on the input pins INP and INM. For DC inputs between 3.6V and 3.8V, a 25Ω resistor is required in series with the input pins. For inputs above 3.8V, the device can handle only transients, which need to have less than 5% duty cycle of overstress. The input pins connect internally to an ESD diode to AV_{DD}, as well as a switched capacitor circuit. The sampling capacitor of the switched capacitor circuit connects to the input pins through a switch in the sample phase. In this phase, an input larger than 2.65V would cause the switched capacitor circuit to present an equivalent load of a forward biased diode to 2.65V, in series with a 60Ω impedance. Also, beyond the voltage on AV_{DD}, the ESD diode to AV_{DD} starts to become forward biased.

In the phase where the sampling switch is off, the diode loading from the input switched capacitor circuit is disconnected from the pin, while the ESD loading to AV_{DD} is still present.

CAUTION:

A violation of any of the previously stated conditions could damage the device (or reduce its lifetime) either due to electromigration or gate oxide integrity. Care should be taken not to expose the device to input over-voltage for extended periods of time as it may degrade device reliability.

POWER-SUPPLY SEQUENCE

The preferred mode of power-supply sequencing is to power-up AV_{DD} first, followed by DRV_{DD}. Raising both supplies simultaneously is also a valid power supply sequence. In the event that DRV_{DD} powers up before AV_{DD} in the system, AV_{DD} must power up within 10ms of DRV_{DD}.

POWER-DOWN

The device will enter power-down mode in one of two ways: either by reducing the clock speed to between DC and 1MHz, or by setting a bit through the serial programming interface. If reducing the clock speed, power-down may be initiated for any clock frequency below 10MHz. The actual frequency at which the device powers down varies from device to device.

The device can be powered down by programming the internal register (see *Serial Programming Interface* section). The outputs become tri-stated and only the internal reference is powered up to shorten the power-up time. The Power-Down mode reduces power dissipation to a minimum of 180mW.

REFERENCE CIRCUIT

The ADS5521 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1µF decoupling capacitor in series with a 1Ω resistor, as shown in Figure 43. In addition, an external 56.2kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 43. No capacitor should be connected between pin 31 and ground; only the 56.2kΩ resistor should be used.

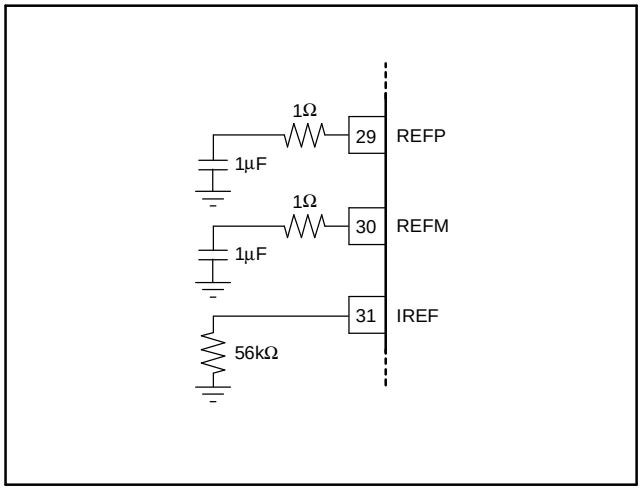


Figure 43. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5521 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal 5kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 44.

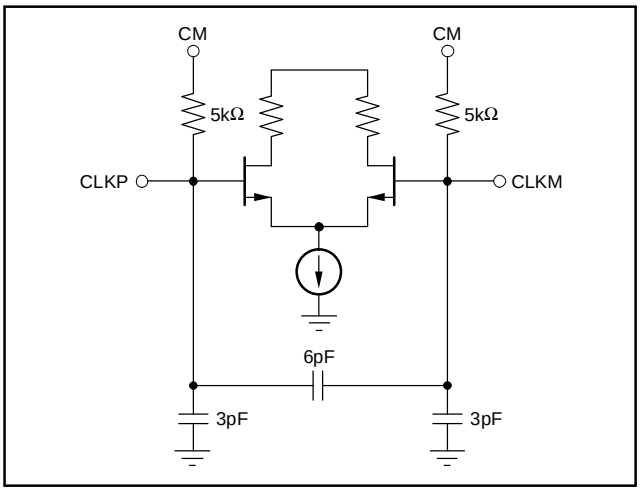


Figure 44. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a 0.01µF capacitor, while CLKP is AC-coupled with a 0.01µF capacitor to the clock source, as shown in Figure 45.

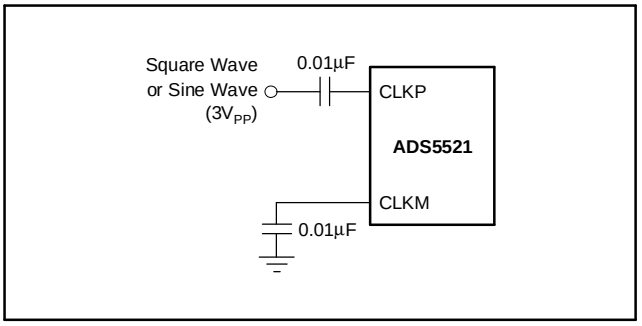


Figure 45. AC-Coupled, Single-Ended Clock Input

The ADS5521 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01µF capacitors, as shown in Figure 46.

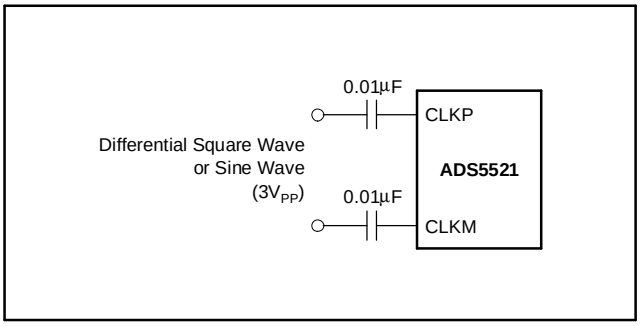


Figure 46. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 47 shows the performance variation of the ADC versus clock duty cycle.

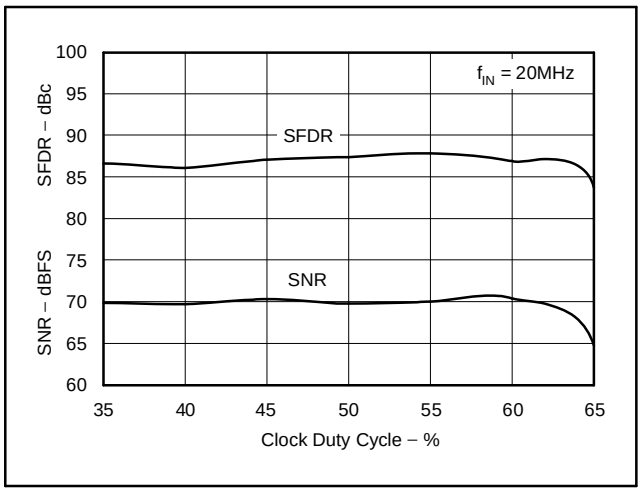


Figure 47. AC Performance vs Clock Duty Cycle

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter will further improve as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 48 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, refer to the ADS55xxEVM User's Guide (SLWU010), available for download from www.ti.com.

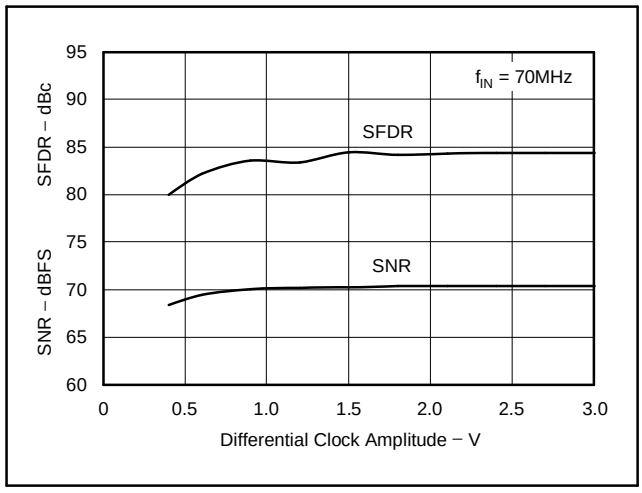


Figure 48. AC Performance vs Clock Amplitude

INTERNAL DLL

In order to obtain the fastest sampling rates achievable with the ADS5521, the device uses an internal digital phase lock loop (DLL). Nevertheless, the limited frequency range of operation of DLL degrades the performance at clock frequencies below 60MSPS. In order to operate the device below 60MSPS, the internal DLL must be shut off using the DLL OFF mode described in the *Serial Interface Programming* section. The Typical Performance Curves show the performance obtained in both modes of operation: DLL ON (default), and DLL OFF. In either of the two modes, the device will enter power-down mode if no clock or a slow clock is provided. The limit of the clock frequency where the device will function properly is ensured to be over 10MHz.

OUTPUT INFORMATION

The ADC provides 12 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals 1 when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to put the outputs into a high-impedance state.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0xFFF in straight offset binary output format, and 0x7FF in two's complement output format. For a negative input overdrive, the output code is 0x000 in straight offset binary output format, and 0x800 in two's complement output format. These outputs to an overdrive signal are ensured through design and characterization.

The output circuitry of the ADS5521, by design, minimizes the noise produced by the data switching transients, and, in particular, its coupling to the ADC analog circuitry. Output D2 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1. Care should be taken to ensure that all output lines (including CLKOUT) have nearly the same load as D2 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. Placing external resistors in series with the outputs is ***not*** recommended.

The timing characteristics of the digital outputs change for sampling rates below the 105MSPS maximum sampling frequency. Table 5 and Table 6 show the setup, hold, input clock to output data delays, and rise and fall times for different sampling frequencies with the DLL on and off, respectively.

Table 7 and Table 8 show the rise and fall times at additional sampling frequencies with DLL on and off, respectively.

To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay, t_d, that results in the desired setup or hold time. Use either of the following equations to calculate the value of t_d.

Desired setup time = $t_d - t_{START}$

Desired hold time = $t_{END} - t_d$

Table 5. Timing Characteristics at Additional Sampling Frequencies (DLL ON)(1)

f_S (MSPS)	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	2.8	3.7		2.8	3.3			0.5	1.7	5.3	7.9			5.8	6.6		4.4	5.3
65	3.8	4.6		3.6	4.1			–0.5	0.8	5.3	8.5			6.7	7.2		5.5	6.4

Table 6. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)(1)

f_S (MSPS)	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	3.2	4.2		1.8	3			3.8	5	8.4	11			5.3	6.6		4.4	5.3
65	4.3	5.7		2	3			2.8	4.5	8.3	11.8			6.6	7.2		5.5	6.4
40	8.5	11		2.6	3.5			–1	1.5	8.9	14.5			7.5	8		7.3	7.8
20	17	25.7		2.5	4.7			–9.8	2	9.5	21.6			7.5	8		7.6	8
2	284	370		8	19			-316	-185	15	76			50	82		75	150

Table 7. Timing Characteristics at Additional Sampling Frequencies (DLL ON)(1)

f_S (MSPS)	CLKOUT t_{RISE} (ns)			CLKOUT t_{FALL} (ns)			CLKOUT t_{JIT} (ps_{PP})		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315
65		3.1	3.5		2.6	2.9		260	380

Table 8. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)(1)

f_S (MSPS)	CLKOUT t_{RISE} (ns)			CLKOUT t_{FALL} (ns)			CLKOUT t_{JIT} (ps_{PP})		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315
65		3.1	3.5		2.6	2.9		260	380
40		4.8	5.3		4	4.4		445	650
20		8.3	9.5		7.6	8.2		800	1200
2		31	52		36	65		2610	4400

(1) Input clock to CLKOUT delay variation can be estimated using the t_{START}, t_{END}, t_{SETUP}, t_{HOLD} numbers in the timing table as:
t_{PDI} (max) = t_{START} (max) + t_{SETUP} (min)
t_{PDI} (min) = t_{END} (min) – t_{HOLD} (min)
Range of t_{PDI} = t_{PDI} (max) – t_{PDI} (min)
These equations are valid for both DLL ON and OFF modes.

SERIAL PROGRAMMING INTERFACE

The ADS5521 has internal registers that enable the programming of the device into modes as described in previous sections. Programming is done through a 3-wire serial interface. The timing diagram and register settings in the *Serial Programming Interface* section describe the use of this interface.

Table 2 shows the different modes and the bit values to be written to the register to enable them.

The ADS5521 internal registers default to all zeros on reset. The device is reset by applying a high pulse on RESET (pin 35) for a minimum of 2µs at least 10ms after both the AV_{DD} and DRV_{DD} power supplies have come up (as illustrated in Figure 2). In reset, the ADC outputs are forced low. Note that the RESET pin has a 200kΩ pull-up resistor to AV_{DD}.

If the ADS5521 is to be used solely in the default mode set at reset, the serial interface pins can be tied to fixed voltages. In this case, tie SCLK high, SEN low, and SDATA to either a high or low voltage.

PowerPAD PACKAGE

The PowerPAD package is a thermally-enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the *Mechanical Data* section.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, please refer to either Application Brief SLMA004B (*PowerPAD Made Easy*), or Technical Brief SLMA002 (*PowerPAD Thermally Enhanced Package*), both available for download at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS5521IPAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5521IPAPG4	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5521IPAPR	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5521IPAPRG4	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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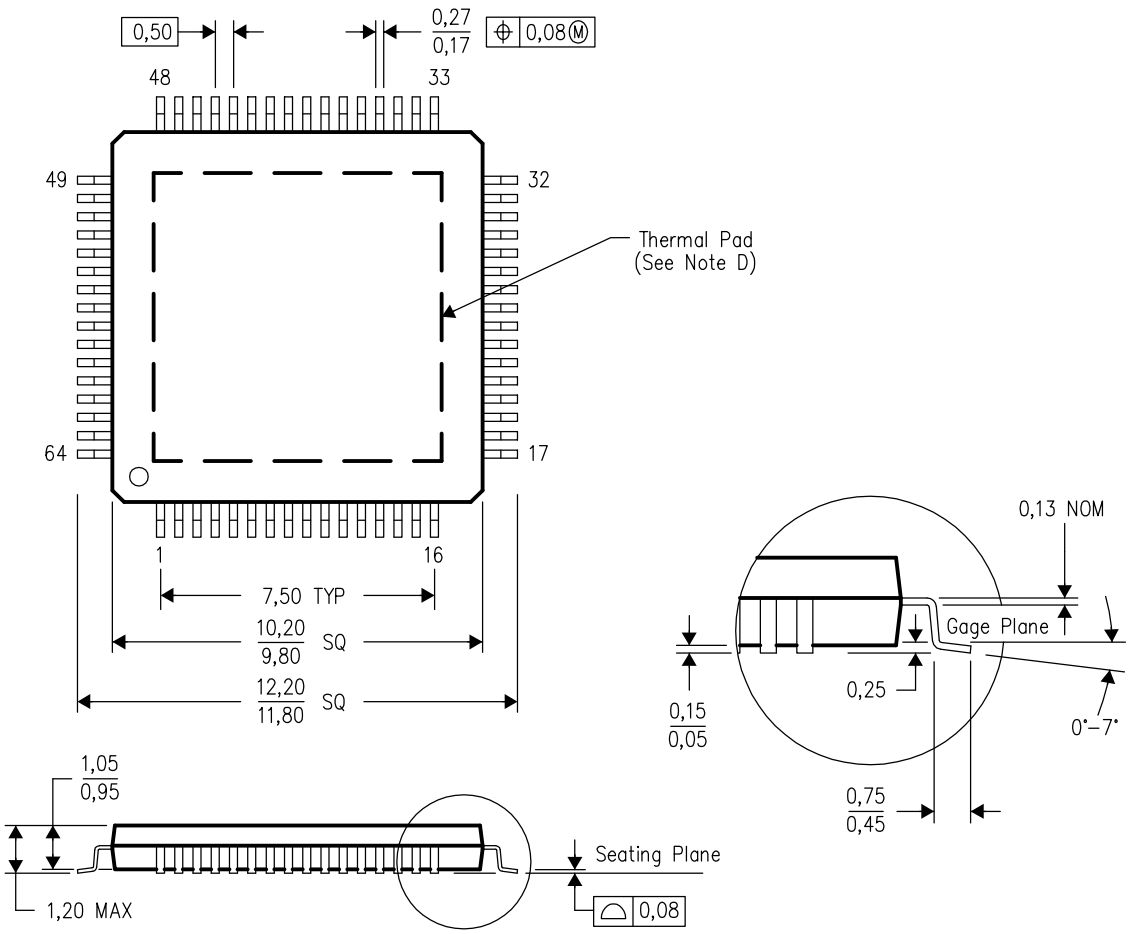
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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